R13

Code No: 113BU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, February/March - 2016

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A [25 Marks]

1.a) Determine the possible base of the numbers in the operation 302/20=12.1. [2]
b) Reduce the expression A'B(D'+C'D)+B(A+A'CD) to one literal. [3]
c) What are static hazards ? [2]
d) Construct full adder using decoder. [3]
e) What is the difference between characteristic table and excitation table? [2]
f) Show the characteristic equation for the true output of JK flip-flop is Q(t+1)=JQ'+K'Q [3]
g) How many bit counter is needed to to provide a clock with cycle time of 50ns if the clock generator produces pulses at a frequency of 80 MHz? [2]
h) Compare Synchronous and Asynchronous counters. [3]
i) What are compatible states? [2]
j) Explain the difference between ASM and conventional flow chart with respect to timing. [3]

PART- B [50 Marks]

2.a) State De-Morgan laws.
b) Perform the following arithmetic operations in binary using signed 2's complement representation for negative numbers (i) (+62) + (-23) (ii) (-62) - (-23).
c) Encode the information character 01101110101 according to the 15 bit Hamming. [2+4+4]

OR

3.a) Obtain the 1's and 2's complement of the binary numbers 10000000 and 0000001.
b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
c) Obtain the truth-table of the function (xy+z)(y+xz) and express the function in sum of min terms and product of max terms. [2+4+4]

4.a) For the function $F(w,x,y,z)=\sum(1,2,3,5,13) + \sum\varphi(6,7,8,9,11,15)$, find the minimal sum of products and product of sums expression.
b) Implement the function $F(A,B,C,D)=\sum(0,1,3,4,6,8,15)$ using 4x1 MUX. [5+5]

OR

5.a) Design a 3-input majority circuit using Multiplexer whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise.
b) Find the min terms of the function wxy+x'z'+w'xz by plotting the function in a map. [5+5]

6.a) Compare Sequential and Combinational circuits.
b) Design a JK flip-flop using Dflipflop. 2-to-1 line MUX and inverter. [4+6]

OR

7.a) What is the difference between a latch and flip-flop?

b) Explain the positive edge triggered D flip-flop with asynchronous reset. [4+6]

8.a) A sequential circuit with two D flip-flops A and B, two inputs x and y; and one output z is specified by A(t+1)=x'y+xA, B(t+1)=x'B+xA, z=B. Draw the logic diagram and list the state table. Draw the state diagram.

b) What is a universal shift register? [8+2]

OR

9.a) Design a counter using T flip-flops with repeated sequence 0,1,3,7,6,4.

b) Show that a Johnson counter with n flip-flops produces a sequence of 2n states. [5+5]

10.a) Draw the multilevel NAND circuit for expression $F = (AB' + CD')E + BC(A + B)$

b) Reduce the given expression to a minimum number of literals:

i) $\overline{(BC' + A'D)}\ \overline{(AB' + CD')}$

ii) $AB' + CD\overline{(A + B)}$. [5+5]

OR

11.a) Find the equivalence partition and corresponding reduced machine in standard form.

PS	NS,Z	
	x=0	x=1
A	F,0	B,1
B	G,0	A,1
C	B,0	C,1
D	C,0	B,1
E	D,0	A,1
F	E,1	F,1
G	E,1	G,1

b) Explain the control implementation using MUX. [6+4]

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Code No: 113BU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, November - 2015

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A **(25 Marks)**

1.a) Convert $(FFF)_H = (\quad)_{10}$. [2M]
b) Draw the 1-bit comparator diagram with logic diagram. [3M]
c) Implement 1-bit Full adder using gates. [2M]
d) Implement one bit half subtractor using Gates. [3M]
e) Draw the excitation table of JK Flip Flop. [2M]
f) Write the excitation table of D flip flop. [3M]
g) Define state diagram. [2M]
h) Define FSM. [3M]
i) How are asynchronous sequential machine characterized? [2M]
j) What is the difference between Mealy and Moore Models? [3M]

PART-B **(50 Marks)**

2.a) Solve the following:
i) $(27.125)_{10} = (\quad)_8$
ii) $(10.6875)_{10} = (\quad)_2$
iii) $(237.75)_8 = (\quad)_{10}$
b) Obtain the complement of the following Boolean expressions
i) A′B+A′BC′+A′BCD+A′BC′D′E
ii) A+B+A′B′C. [5+5]

OR

3.a) Encode the decimal numbers into:
i) $(56)_{10} = (\quad)$ Gray code
ii) $(20.305)_{10} = (\quad)$ Excess-3 code
iii) $(32.89)_{10} = (\quad)$ BCD code
b) Realize the following logic function using only NAND gates
$f(a,b,c,d) = \Sigma(0,2,4,6,9,11,13,15)$. [5+5]

4.a) Minimize the following function using K-map.
$f(A,B,C,D) = \Sigma_m(0, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 13)$
b) Minimize the following expression using K-map and realize using NOR gates. $f(A,B,C,D) = \prod M(1, 2, 3, 8, 9, 10, 11, 15)$. [5+5]

OR

5.a) Determine the prime implicants of the function.
$f(W,X,Y,Z) = \Sigma(1,4,6,7,8,9,10,11,15)$. Also minimize the logic function using Tabulation method.
b) Implement the following logic function using 16:1 Multiplexer and 8:1 Multiplexer.
$f(a,b,c,d) = \Sigma(0,3,4,8,9,15)$. [5+5]

6.a) Explain the techniques used to eliminate racing condition in JK flip flops.
b) Design a S-R latch using 2-input NAND gates. [5+5]

OR

7.a) Convert a clocked S-R flip flop to a T-flip flop.
b) Explain the design of a clocked Flip-Flop. [5+5]

8.a) Design a 4-bit binary UP/DOWN ripple counter.
b) What are the different types of registers? Explain the Serial Input Parallel Output Shift register. [5+5]

OR

9.a) Explain the operation of RS-clocked flip-flop with logic diagram. Show the relevant waveforms.
b) Design a mod-10 Ripple counter using T flip flops and explain its operation. [5+5]

10.a) Discuss about completely and incompletely specified sequential machines.
b) What are State Machine charts? What are the principal components of State Machine chart? [5+5]

OR

11.a) Implement a weighing machine with the help of SM Chart.
b) Draw the typical flow chart, State Machine chart and state graph diagrams. [5+5]

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Code No: 54010 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, May - 2015
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Explain the procedure for converting Gray code to Binary code with an example.
b) Solve for X
i) $(F3A7C2)_{16} = (X)_{10}$
ii) $(2AC5)_{16} = (10949)_X$
iii) $(0.93)_{10} = (X)_8$
iv) $(4057.06)_8 = (X)_{10}$ [7+8]

2.a) Write the Dual of
i) (A+BC'+AB)
ii) (AB+B'C+CD)
b) Prove the following identity
XY + X'Y' +YZ = XY +X'Y' +X'Z. [8+7]

3. Use tabular procedure to simplify the given expression
f(v,w,x,y,z) =∑m(0,4,12,16,19,24,27,28,29,31) in SOP form and draw the circuit using only NAND gates. [15]

4.a) Design a logic circuit to encode a 2^n input bits to n bit output.
b) Design a 4 bit Parallel adder using full adders. [8+7]

5. Design a sequential logic circuit of a 4 bit counter to start counting from 0000 to 1000 and this process should go on. Draw the ASM chart and design the Data processing unit and the control unit. [15]

6.a) Draw the block diagram of a ROM. Define address and word. Relate the number of output lines with number of bits in a word. How an output word can be selected?
b) For a 64×8 ROM, determine the number of words it contains and the size of each word. How many output lines are there for the ROM? [7+8]

7.a) Give a detailed comparison between combinational logic circuits and sequential logic circuits.
b) Explain the operation of JK flip flop with the help of input output waveforms. [8+7]

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Code No: 113BU

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, May/June - 2015

SWITCHING THEORY AND LOGIC DESIGN

(Common to ECE, EIE)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks.

PART- A

(25 Marks)

1.a) Find the complement of (AB'+C)D'+E. [2M]
b) What are single error detecting codes and how error detection is accomplished? [3M]
c) What are static hazards? [2M]
d) Explain the six variable Karnaugh map. [3M]
e) Define sequential circuit and give example. [2M]
f) Explain about clocked T flip-flop. [3M]
g) What is the difference between synchronous and asynchronous Sequential circuits? [2M]
h) A 3-bit binary ripple counter uses T -flip-flops that trigger on the negative edge of the clock. What will be the count if complement outputs of the flip-flop are connected to the clock? Draw the timing waveform. [3M]
i) What is the difference between flow chart and ASM chart? [2M]
j) What are the capabilities of finite state machine? [3M]

PART-B

(50 Marks)

2.a) Find the 16's complement of AF3B.
b) Formulate a weighted binary code for the decimal digits using weights 6,3,1,1.
c) Implement F=(AB'+A'B)(C+D') using NAND gates. [2+4+4]

OR

3.a) Convert decimal 9126 to both BCD and ASCII codes.
b) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.
c) Express the complement of $F(A,B,C,D)=\sum(0,2,6,11,13,14)$ in sum of min terms. [2+4+4]

4.a) Use the tabulation procedure to generate the set of prime implicants and to obtain all minimal expressions for the function:
$F(w,x,y,z)=\sum(0,1,4,5,6,7,9,11,15) + \sum\varphi(10,14)$
b) Implement the function $F(A,B,C,D)=\sum(0,1,3,4,6,8,15)$ using required capacity decoder and logic gates. [5+5]

OR

5.a) Design a BCD adder.
b) Find all the prime implicants for the Boolean function:
$F(w,x,y,z)=\sum(1,3,4,5,10,11,12,13,14,15)$ and find which are essential. [5+5]

6.a) With a neat diagram explain about D-Type positive edge triggered flip-flop.

b) Design a T flip-flop using JK flip-flop. Use k-maps for the design. [5+5]

OR

7.a) What is the difference between edge triggering and level triggering? Explain about Edge triggered JK flip-flop with a neat diagram.

b) Design a JK flip-flop using SR flip-flop. Use k-maps for the design. [5+5]

8.a) Design a sequential circuit with two D flip-flops A and B, and one input x. When x=0, the state of the circuit remains same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

b) List the basic types of shift registers in terms of data movement. [8+2]

OR

9.a) Design a divide by 6 ripple counter using T flip-flops.

b) Design a counter using JK flip-flops with the repeated binary sequence 0,1,2,3,4,5,6. [5+5]

10.a) Explain the state minimization using merger graph and merger table.

b) Explain the multiplexer method of implementing ASM charts. [5+5]

OR

11.a) Determine the minimal state table equivalent to the state table given:

PS	NS,Z	
	x=0	x=1
A	A,1	E,0
B	A,0	E,0
C	B,0	F,0
D	B,0	F,0
E	C,0	F,1
F	C,0	F,1
G	D,0	H,1
H	D,0	H,1

b) Draw the ASM chart and state table for a 2-bit counter having one enable line E such counting is enabled when E=1 and counting is disabled when E=0. [5+5]

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R09

Code No: R09220204

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

B.Tech II Year II Semester Examinations, May-2013

Switching Theory and Logic Design

(Common to EEE, ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

- - -

1.a) Convert the decimal number 234 to binary, octal and hexadecimal number systems.

b) Find the canonical product-of-sums form for the function $F(x,y,z) = x'y' + z'x'$

c) Find the sum of -8 + 2 using signed 2's complement representation. (5+5+5)

2.a) Prove the following identity $xy + x'y' + yz = xy + x'y' + x'z$.

b) Simplify the given function $F(w, x, y, z) = \Sigma (0, 1, 2, 3, 4, 6, 7)$ to minimum number of literals. (6+9)

3.a) For the given function $F(w, x, y, z) = \Sigma (0, 1, 2, 3, 4, 6, 7, 9, 11, 15)$

i) Show the K-map

ii) Find all prime implicants and indicate which are essential.

iii) Find a minimal expression for F and realize using basic gates. Is it unique?

b) Design a 16x1 multiplexer using 4x1 multiplexers only. (10+5)

4. Use tabulation procedure to generate the prime implicants and essential prime implicants and to obtain all minimal expression for the given function $F(A, B, C, D) = \Sigma (1, 5, 6, 12, 13, 14) + d (2, 4)$. (15)

5.a) Define static hazard. Illustrate with example.

b) Design a combinational circuit that converts the given binary number to excess-3 code. (6+9)

6.a) Design a mod-10 counter using JK flip-flops.

b) Write the characteristic table, characteristic equations and excitation table for RS, T and D flip-flops. (7+8)

7.a) Illustrate the completely specified function with example. Write a procedure to design completely specified functions.

b) Define the terms primitive flow table and reduced flow table. (10+5)

8. Write short notes on

a) Incompletely specified functions

b) Asynchronous state machines

c) Logic synthesis. (5+5+5)

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Code No: 07A4EC09 **R07**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD

B.Tech II Year II Semester Examinations, May-2013

Switching Theory and Logic Design

(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 80**

Answer any five questions

All questions carry equal marks

- - -

1.a) Convert the hexadecimal number AE28 to octal, binary and decimal number systems.

b) State and Prove Huntington postulates. (7+9)

2.a) State and prove the Demorgan's theorem

b) Simplify the given function F(w, x, y, z) = Σ (0, 12, 13, 14, 15) using Boolean theorems to minimum number of literals. (7+9)

3.a) For the given function F(w, x, y, z) = Σ (0, 1, 2, 3, 6, 7, 9, 11, 15)

i) Show the K-map

ii) Find all prime implicants and indicate which are essential.

iii) Find a minimal expression for F and realize using NAND gates. Is it unique?

b) Implement the Function x'y + y'z using 2×1 multiplexer only. (10+6)

4. Use tabulation method to generate the prime implicants and essential prime implicants and to obtain all minimal expression for the given function F(A, B, C, D) = Σ (0, 1, 2, 4, 5, 12, 13, 14) + d (6, 15). (16)

5.a) Realize the Full adder using NAND gates only.

b) Design a combinational circuit that converts the binary number to gray code. (7+9)

6.a) Design Mod-10 counter using JK flip-flops.

b) Write the characteristic table, characteristic equations and excitation table for RS, T and D flip-flops. (8+8)

7.a) Illustrate a incompletely specified function with example. Write a procedure to simplify the incompletely specified function to minimum number of literals.

b) Define the terms prime implicant and essential prime implicant. Give example for each. (8+8)

8.a) Design a combinational circuit to generate a parity generator circuit.

b) Write a procedure to identify whether a given function is symmetric or not. (8+8)

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Code No: 134CF **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, April - 2018

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) What is self complementing code? Give example. [2]
b) State and Prove Demorgan's theorem. [3]
c) What are Hazards? List their types. [2]
d) Design 2 × 1 Multiplexer with neat logic diagram. [3]
e) Write the characteristic table of JK Flip flop. [2]
f) Draw the logic diagram of Master-Slave D flip flop. Use NAND gates. [3]
g) What is switch tail ring counter? [2]
h) What is a Ring Counter? What are applications of Ring counters? [3]
i) What is an ASM Block? [2]
j) Define merger graph of n-state machine M. [3]

PART-B

(50 Marks)

2.a) i) Convert the given Octal number $(2564.603)_8$ to Hexadecimal Number.
ii) Given that $(81)_{10} = (100)_b$, Find the value of b.
b) Encode data bits 1101 into 7 bit even parity Hamming Code. [5+5]

OR

3.a) Prove that AB'C + B + BD'+ ABD'+ A'C = B + C.
b) Simplify the following expression F = AB'+ABD+ABD'+A'C'D'+A'BC' and implement with NAND gates. [5+5]

4.a) Design a code converter that converts BCD messages into Excess-3 code. The converter has four input lines carrying signals labeled *w*, *x*, *y* and *z* and four output lines carrying signals *f*1, *f*2, *f*3, and *f*4.
b) Simplify the following Boolean expression using K- map and implement them with NOR logic gates
$F(A,B,C,D) = \Sigma m(1,3,7,11,15) + d(0,2,5)$ [5+5]

OR

5.a) Design and explain 3 to 8 decoder with necessary truth table and logic diagram.
b) Write short notes on Hazards and Hazard free relations. [5+5]

6.a) Derive the characteristic equation for JK flip-flop and T flip-flop.
b) Distinguish combinational and sequential circuits. [5+5]

OR

7.a) What are the fundamentals of Sequential machine operation?
b) Discuss about binary cell in detail. [5+5]

8.a) Design a 4-bit binary synchronous counter with D flip flops.
b) What are the steps in state reduction? Explain with an example. [5+5]

OR

9.a) Construct a Johnson counter for 10 timing signals.
b) Draw the 4-bit binary ripple counter using flip flops that trigger on positive edge transition. [5+5]

10.a) Draw the Merger Graph and obtain the set of maximum compatibilities for the given incompletely specified sequential machine.

Present State	Next State, Z	
	I_1	I_2
A	E, 0	B, 0
B	F,0	A, 0
C	E, _	C, 0
D	F, 1	D, 0
E	C,1	C,0
F	D,-	B,0

b) Draw the State diagram, State table and ASM chart for a D flip-flop. [5+5]

OR

11.a) Draw the State diagram and ASM chart for sequence detector to detect 1010.
b) We wish to design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line.
i) Find the state diagram.
ii) Determine the type of the circuit (Moore or Mealy model). [5+5]

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Code No: 123BU **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, November/December - 2016
SWITCHING THEORY AND LOGIC DESIGN
(Common to ECE, EIE, ETM)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A **(25 Marks)**

1.a) What are the different illegal states of BCD and XS-3? [2]
b) State and prove the included factor theorem. [3]
c) What is the prime implicant chart? [2]
d) Draw the full subtractor using X-OR and AOI gates. [3]
e) Define the Propagation delay time. [2]
f) Draw the conversion table of SR flipflop to JK flipflop. [3]
g) Define the ring counter. [2]
h) What are the applications of Shift register? [3]
i) What are the capabilities of FSM? [2]
j) Draw the state box and Decision box diagrams of ASM Charts. [3]

PART-B **(50 Marks)**

2.a) Convert the gray number 10110101 into:
i) Decimal ii) Octal iii) Hex
b) Perform the subtraction in BCD using 9's complement method for 592.6-887.9. [5+5]

OR

3.a) Derive the Boolean expression for a two input Ex-OR gate to realize with the two input NAND gates without using complemented variables and draw the circuit.
b) Expand (A+D')(A+C')(A'+B)(A'+B+C) into maxterms and minterms. [5+5]

4.a) Using the QM method, obtain the simplified expression for:
F=Σm (4,5,6,7,8,9,)+d(10,11,12,13,14,15).
b) Give the limitations of K-mapping method. [5+5]

OR

5.a) Design the 8:1 MUX for the given Boolean Expression f=Σm(1,3,4,11,12,13,14,15).
b) Design a combinational circuit to detect the decimal numbers 0,2,4,6 and 8 in a 4-bit XS-3 code input. [5+5]

6.a) Explain the generation of narrow spikes in the edge triggered flip-flops.
b) Draw and explain the operation of the Master Slave SR flip-flops with block diagram. [5+5]

OR

7.a) Derive the characteristic equation of JK flip-flop from the Excitation table.
b) Explain the Race around condition in flip-flops in detail. [5+5]

8.a) Design a Ring counter using shift register.
b) Define state, state diagram. Draw state diagram taking any one as an example. [5+5]

OR

9.a) Design a counter circuit for a mod-asynchronous counter using JK flip-flops.
b) Design a 3-bit up/down counter which counts up when the control signal M=1 and counts down when M=0. [5+5]

10. Draw the merger graph and obtain the set of Maximal compatibles for the incompletely specified sequential machine for given state table. [10]

PS	NS,Z	
	I1	I2
A	E,0	B,0
B	F,0	A,0
C	E,--	C,0
D	F,1	D,0
E	C,1	B,0
F	D,--	B,0

OR

11.a) Draw and explain the data path subsystem for weighing machine.
b) Draw the State diagram, state table and ASM chart for a D flip-flop. [5+5]

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